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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,997	11/02/2001	Partha P. Tirumalai	SUN-P7005-RA	1272

22835 7590 05/19/2006

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EXAMINER

FOWLKES, ANDRE R

ART UNIT	PAPER NUMBER
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2192

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<p align="center">Office Action Summary</p>	Application No. 10/052,997		Applicant(s) TIRUMALAI ET AL.	
	Examiner Andre R. Fowlkes		Art Unit 2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 February 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____. | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
6) <input type="checkbox"/> Other: _____. |
|--|--|

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/27/06 has been entered.

2. Claims 1-21 are pending. Claims 1, 8, 14 and 15 have been amended.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Santhanam, U.S. Patent No. 5,704,053 in view of Wu, et al., (Wu), U.S. Patent Publication No. 2003/0066061 (art made of record).

As per claim 1, Santhanam discloses a **method for generating code to perform anticipatory prefetching for data references**, (col. 3:47-49, "The current

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invention provides a new compiler for such a processor that facilitates efficient insertion of explicit data prefetch instructions into loops within application programs”),

comprising:

- receiving code to be executed on a computer system; analyzing the code to identify data references to be prefetched, wherein data references are identified from basic blocks within *if* conditions regardless of whether the basic blocks are likely to execute, (col. 5:14-16, “Simple subscript expression analysis is used to determine data prefetching requirements, as opposed to sophisticated reuse/dependence analysis”, simple subscript expression analysis analyzes all basic blocks and does not rely on profile data and therefore does not preclude the analysis of certain blocks based on profile information, and col. 5:26-28, “Execution profiles from previous runs of an application are exploited in the insertion of prefetch instructions”, this statement indicates that use of profile data, in certain embodiments, but does not disclose precluding the analysis of basic blocks that are not likely to execute, and col. 10:42-45, “Global optimizations include code improving transformations that are applied based on analysis that spans across basic block boundaries.”), **and wherein analyzing the code involves:**

- performing a first marking phase in which only data references located in blocks that are certain to execute are considered in determining which data references are covered by preceding data references (col. 17:25-30, “a two-pass strategy is used... In the first pass, it is necessary to identify clusters of adjacent references... The distinguishing feature of each such cluster

is that the references within the cluster share group spatial locality (i.e. data references that cover each other are determined)", and col. 12:18-22, "(Only memory references (that are certain to execute are) ... analyzed for data prefetching purposes"),

- performing a second marking phase in which data references that are located in blocks that are not certain to execute are considered (col. 18:39-41, "Having identified the cluster leaders (i.e. the preceding references that cover other references), in the first pass, in the second pass, the algorithm attempts to exploit temporal locality between the clusters (i.e. references)", and col. 14:6-7, "Now it is also necessary to address the issue of loops that have internal branches"),

- inserting prefetch instructions into the code in advance of the identified data references based upon code analysis (col. 3:51-53, "Analysis and explicit data cache prefetch instruction insertion are performed by the compiler"), **wherein inserting prefetch instructions includes inserting multiple redundant prefetch instructions for a given data reference** (col. 6:61-62, "the system is issuing a redundant (prefetch) instruction(s) to the memory system to retrieve the same cache line (i.e. data reference)"),

- wherein inserting multiple redundant prefetch instructions involves inserting the multiple redundant prefetch instructions into unused instruction slots and wherein executing multiple redundant prefetch instructions potentially avoids a cache miss (col. 6:56-67, "some of the prefetches are redundant ... Typically,

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computer systems that support this type of prefetch instruction track the instructions to determine if a requested address to prefetch a cache line matches a later prefetch to the same cache line. In such event, the second prefetch request to main memory is dropped (in other cases, multiple prefetch instructions are executed”).

Santhanam doesn't explicitly disclose:

- **calculating a prefetch ahead distance, wherein the prefetch ahead distance includes the ratio of outstanding prefetches to the number of prefetch streams**
- **optimizing code based upon the prefetch ahead distance.**

However, Wu in an analogous environment, discloses:

- **calculating a prefetch ahead distance, wherein the prefetch ahead distance includes the ratio of outstanding prefetches to the number of prefetch streams** (para. 82:5-10, “If the frequency ratio of load instruction (i.e. the prefetch ahead distance) exceeds a predefined threshold, ...(the) load instruction can be (optimized)”),
- **optimizing code based upon the prefetch ahead distance** (para. 82:1-2, “FIG. 8 illustrates the transformation of program code (i.e. optimization) based on load value specialization (i.e. a prefetch ahead distance ratio)”).

Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the teachings of Wu into the system of Santhanam to have a optimization of code based on a prefetch ratio. The modification would have been obvious because one of ordinary skill in the art would have wanted to use well known and well document code analysis & optimization techniques to increase the effectiveness of computer systems which utilize prefetch instructions.

As per claim 2, the rejection of claim 1 is incorporated and further, Santhanam discloses:

- **profiling execution of the code to produce profiling results** (col. 14:8-10, "using previously collected execution profile information, which indicates the execution count for each basic block"),

- **using the profiling results to determine whether a given block of instructions is executed frequently enough to perform the second marking phase on the given block of instructions** (col. 14:6-10, "Now, it is also necessary to address the issue of loops that have internal branches. The minimum loop iteration latency for such loops is estimated by using previously collected execution profile information, which indicates the execution count for each basic block in the loop body.").

As per claim 3, the rejection of claim 2 is incorporated and further, Santhanam discloses that **determining whether the given block of instructions is executed frequently enough to perform the second marking phase involves comparing a**

frequency of execution for the given block from the profiling results with a threshold value indicating a minimum frequency of execution to be considered in the second marking phase (col. 12:18-22, "(Only) memory references with (a minimum stride value) ... are further analyzed for data prefetching purposes").

As per claim 4, the rejection of claim 1 is incorporated and further, Santhanam discloses that analyzing the code involves **identifying loop bodies within the code and identifying data references to be prefetched from within the loop bodies** (col. 8:30-35, "One important feature of the invention identifies loops and access patterns to allow a determination of how many cycles are devoted to loop iterations, and therefore allows insertion of the prefetch instruction(s)").

As per claim 5, the rejection of claim 4 is incorporated and further, Santhanam discloses that **if there exists a nested loop within the code**, (col. 16:60, "consider the following 'C' loop nest"), **analyzing the code involves:**

- **examining an innermost loop in the nested loop** (col. 17:5-6, "(the) inner j-loop (is examined)"),

- **examining a loop outside the innermost loop if the innermost loop is smaller than a minimum size or is executed fewer than a minimum number of iterations** (col. 17:8-9, "It must be determined whether it is sufficient to insert only one prefetch instruction on behalf of (inner and outer loop references if the inner loop is executed fewer than a minimum number of iterations)").

As per claim 6, the rejection of claim 4 is incorporated and further, Santhanam discloses that **analyzing the code to identify data references to be prefetched involves examining a pattern of data references over multiple loop iterations** (col. 14:7-10, "(Data references to be prefetched are identified) by using previously collected execution profile information, which indicates the execution count for each basic block in the loop body.>").

As per claim 7, the rejection of claim 1 is incorporated and further, Santhanam discloses that **analyzing the code involves analyzing the code within a compiler** (col. 3:47-49, "The current invention provides a new compiler for such a processor that facilitates efficient insertion of explicit data prefetch instructions into loops within application programs").

As per claims 8-14, this is a computer readable medium/product version of the claimed method discussed above, in claims 1-7, wherein all claimed limitations have also been addressed and/or cited as set forth above. For example, see Santhanam, col. 3:47-49 and Wu, para 25:1-26:11 and 82:1-10.

As per claims 15-21, this is an apparatus version of the claimed method discussed above, in claims 1-7, wherein all claimed limitations have also been addressed and/or cited as set forth above. For example, see Santhanam Fig. 1 item 10,

“computer architecture” and associated text and Wu, and Wu, para 25:1-26:11 and 82:1-10.

Response to Arguments

5. Applicants arguments have been considered but they are not persuasive.

In the remarks, the applicant has argued substantially that:

1) Santhanam does not disclose inserting prefetch instructions based on the ratio of outstanding prefetches and the number of prefetch streams, at p. 9:8-10.

Examiner's response:

1) Applicant's arguments with respect to claims 1, 8 and 15 have been considered but are moot in view of the new ground(s) of rejection. The Santhanam/Wu combination discloses inserting prefetch instructions based on the ratio of outstanding prefetches and the number of prefetch streams, at Santhanam, col. 3:47-49 and Wu, para 25:1-26:11 and 82:1-10. Additionally, while the terms “outstanding prefetch” and “prefetch stream” are mentioned in the specification (p. 15:21-23), the examiner suggests that the applicant include the definition of the these terms to aid in future prosecution and provide a clear record.

Conclusion


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6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre R. Fowlkes whose telephone number is (571) 272-3697. The examiner can normally be reached on Monday - Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571)272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ARF



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SUPERVISORY PATENT EXAMINER